Amendments the Specification:

Please replace the BRIEF DESCRIPTION OF THE DRAWING(S) section beginning on page 8 with the following amended BRIEF DESCRIPTION OF THE DRAWING(S) section:

BRIEF DESCRIPTION OF THE DRAWING(S)

[0019] The benefits, features, and advantages of the present invention will become better understood with regard to the following description and accompanying drawings in which:

[0020] FIG. 1 is simplified schematic diagram of a portion of a DC-DC power regulator including a portion of a precision margining circuit implemented according to an exemplary embodiment of the present invention;

[0021] FIG. 2 is a simplified schematic diagram of a portion of the feedback circuit of the regulator of FIG. 1 employing margin control according to an exemplary embodiment of the present invention; and

[0021.1] FIG. 3 is a simplified schematic diagram of a portion of the feedback circuit of the regulator device of FIG. 1 employing margining control according to a more specific embodiment of the present invention.

Amendments to the Specification (continued):

Please replace paragraph [0024] beginning on page 10 with the following amended paragraph [0024]:

[0024] Within the regulator device 100, the margining circuit 101 includes an amplifier 111 having an ~~non-~~inverting input receiving a reference voltage VREF. In one embodiment, VREF is a precision internal bandgap voltage of 0.6V as known to those skilled in the art. The output of the amplifier 111 is coupled to the gate of an N-channel device Q1, such as a metal-oxide semiconductor, field-effect transistor (MOSFET), having its source coupled to a source voltage VCC. The non-inverting input of the amplifier 111 is coupled to the common pole of a first single-pole, double-throw (SPDT) switch SW1 having selectable terminals labeled A and B. The drain of Q1 is coupled to the common pole of a second SPDT switch SW2, also having selectable terminals labeled A and B. The MARCTRL pin 103 is coupled to a control terminal 113 of both switches SW1 and SW2, such that both switches SW1, SW2 select terminal A when MARCTRL is asserted high and terminal B when MARCTRL is asserted low. The A terminal of switch SW1 and the B terminal of switch SW2 are coupled together and to the OFS+ pin 105. The B terminal of switch SW1 and the A terminal of switch SW2 are coupled together and to the OFS- pin 107.